



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,055	07/31/2003	Shahriar Ahmed	42P10970C	3607

7590 04/21/2006

Michael A. Bernadicou  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP  
12400 Willshire Boulevard  
Seventh Floor, CA 90025

EXAMINER
----------

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/633,055		AHMED ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Junghwa M. Im		2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 March 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 13,17-22 and 27-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☒ Claim(s) 13,17-22 and 27-31 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 13, 17-22 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akbar et al. (U.S. Pat. No. 4957875), hereinafter Akbar in view of Hameed et al. (U.S. Pat. No. 5024957), hereinafter Hameed.

Regarding claim 13, Fig. 8 of Akbar shows a bipolar junction transistor comprising:

- in a substrate 32, a first isolation structure 36 spaced apart from a second isolation structure 38;
- a base 14, 22 formed in the substrate;
- an emitter stack 16 disposed above the substrate and between the first isolation structure and the second isolation structure;
- a recess (a portion between the regions 17, 18) disposed immediately adjacent to the emitter stack and disposed between the emitter stack and the first isolation structure, wherein the recess exposes a collector tap 26, wherein the emitter stack and the recess share a boundary; and
- an emitter cut (an emitter/base junction) provided at the bottom of said emitter stack and on top of an intrinsic base structure (a portion of the base in contact with the emitter) formed in the substrate.

Fig. 8 of Akbar shows most aspect of the instant invention except an intrinsic base formed in the epitaxial base. Fig. 9 of Hame shows a semiconductor device wherein an intrinsic base 32 formed in the epitaxial base 32A (col. 4, lines 10-16) is formed in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hame into the device of Akbar in order to have an intrinsic base in the epitaxial base formed in the substrate to alleviate the leakage current.

Note that "epitaxial" is a process designation, and would not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 17, Fig. 8 of Akbar shows a buried layer 34 in the substrate between the first isolation structure and the second isolation structure.

Regarding claim 18, Fig. 8 of Akbar shows a bipolar junction transistor further including: a collector structure 12 disposed in the substrate below the emitter stack; and an intrinsic base structure 14 disposed between the emitter stack 16 and the collector structure 12.

Regarding claim 19, Fig. 8 of Akbar shows a bipolar junction transistor further including: a collector structure 12 disposed in the substrate below the emitter stack; and a dielectric layer 18, 20 disposed above the substrate and below the emitter stack and above the collector structure; and an intrinsic base structure 14 disposed between the emitter stack and the collector structure.

Fig. 8 of Akbar shows most aspect of the instant invention except "the dielectric layer is patterned for said emitter cut to be formed therein." Fig. 9 of Hame shows a semiconductor

Art Unit: 2811

device wherein the dielectric layer 34, 36 is patterned for the emitter cut (a bottom portion of the emitter 40) to be formed therein. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hame into the device of Akbar in order to have to a semiconductor device wherein the dielectric layer patterned for the emitter cut to reduce parasitic capacitance between the emitter and the extrinsic base.

Regarding claim 20, Fig. 8 of Akbar shows a collector tap 26 is N type.

Regarding claim 21, Akbar discloses that the substrate includes a BiCMOS structure (col. 1, lines 11-14).

Regarding claim 22, Fig. 8 of Akbar shows the BJT is selected from a monojunction BJT device and a heterojunction BJT device.

Regarding claim 27, Fig. 8 of Akbar shows the collector tap 127 is self-aligned with the emitter stack.

Also, note that “self-aligned” is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 28, Fig. 8 of Akbar shows the bipolar junction transistor is an NPN transistor, and the collector tap is N type.

Regarding claim 29, Akbar discloses the bipolar junction transistor is a PNP transistor, and the collector tap is P type (col. 3, lines 24-25).

Regarding claim 30, Fig. 8 of Akbar shows the collector tap has no doping that is different from the substrate.

Regarding claim 31, Fig. 8 of Akbar shows the recess is a contact corridor.

***Response to Arguments***

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



**EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800**